

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	9	triple adj polysilicon ti.	USPAT: US-PGPUB	2003/01/14 13:17
2	BRS	L2	10	("4638347" "4639893" "5168465" "5280446" "5408115" "5422504" "5554869" "5502965" "5734607" "5864501").PN	USPAT	2003/01/14 13:19
3	BRS	L10	3	9 and mnos	USPAT: US-PGPUB	2003/01/14 13:27
4	BRS	L9	45	swatt	USPAT: US-PGPUB	2003/01/14 13:27

	Type	Hits	Search Text	DBs	Time Stamp
1	IS&R	363	(257/324) CCLS	USPAT; US-PGPUB	2003/01/14 12:13
2	BRS	21	((257/324) CCLS) and select adj gate	USPAT; US-PGPUB	2003/01/14 12:15
3	BRS	35	mnos and select adj gate	USPAT; US-PGPUB	2003/01/14 12:16
4	BRS	33	(mnos and select adj gate) not (((257/324) CCLS) and select adj gate)	USPAT; US-PGPUB	2003/01/14 12:16

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 5864501 A	6	Test pattern structure for endurance test of a flash memory device	365/185 09	257/316; 257/319; 257/321; 257/48; 365/185.1; 365/185.33	Lee, Hee Youl
2	US 5168465 A	48	Highly compact EPROM and flash EEPROM devices	257/320	257/321; 257/E27 103; 257/E29 302; 257/E29 306; 365/185.03; 365/185.09; 365/185 14; 365/185 15; 365/185.22; 365/185.25; 365/185.27; 365/203	Harari, Eliyahou
3	US 6346725 B1	13	Contactless array of fully self-aligned triple polysilicon, source-side injection, nonvolatile memory cells with metal-overlaid wordlines	257/316	257/900	Ma, Yueh Yale et al